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3 Tutorial on CMOS VLSI

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| Day On My Plate VLSI

Design Module 4 [Part 5]:

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CHAPTER 4 SOLUTIONS 9 effort

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should be about 4. This design has imbalanced delays and excessive efforts. The path effort is $F = 12 * 6 * 9 = 648$. The best number of stages is 4 or 5. One way to speed the circuit up is to add a buffer (two inverters) at the end. The gates should be resized to bear efforts of $f = 648^{1/5} = 3.65$ each.

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International Journal of VLSI design & Communication Systems (VLSICS) Vol.7, No.5/6, December 2016 4 3. CIRCUIT MODEL AND STATIC

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TIMING ANALYSIS The first step in our design methodology is to classify the logic gates of the circuit according to gate type and no. of inputs such as (AND2, AND3, AND4, OR2, etc.) all these gates are

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